

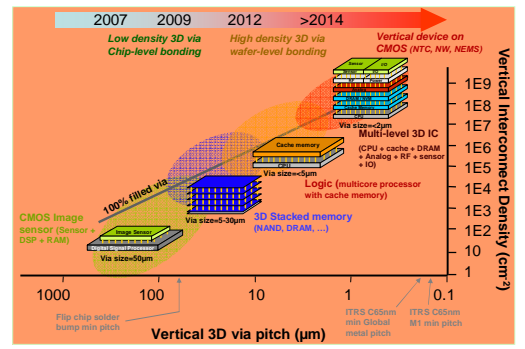


### Context and objectives

**Moore's law scaling**, the reduction of minimum device feature size to improve speed and integration density in planar integrated circuits, is increasingly difficult to continue due to major economic and physical obstacles.

**3D integration**, exploiting the vertical dimension, provides an opportunity to continue to achieve the performance levels predicted by the extrapolation of Moore's law, but using a **different technological approach** and a **major design paradigm shift** towards **equivalent scaling** and **functional diversity** through unconventional approaches.

This **industrial research project** aims to implement an **integrated research approach** to set up the food chain from **3D technology** to **innovative imager applications** via **novel design technology approaches** in order to accelerate the exploitation of the technology to its full potential.



### WP1: Fabrication Technology

Development of generic technological modules mandatory to stack an imager on a signal processing unit (CPU and memory)

**Through Silicon Via (TSV) technology**

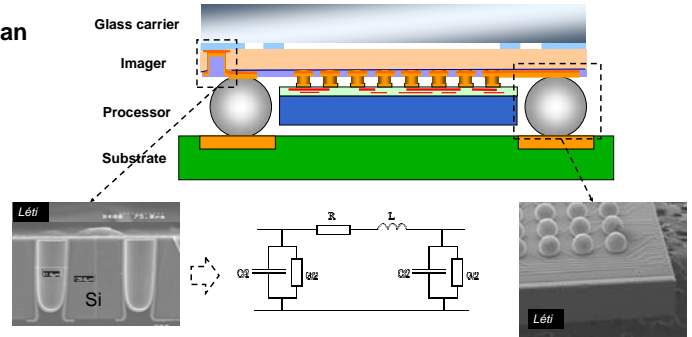
- Elementary process step for demonstrator fabrication
- Technology information for TSV simulation and modeling

**Dies stacking and inter-die interconnects**

- Innovative low temperature micro-interconnects
- Substrate thinning and die to wafer eutectic bonding

**TSV electromagnetic characterization and compact modeling**

- Electromagnetic 3D modeling of TSV vs RF characterization
- Extraction of equivalent electrical models of TSV



### WP2: Design Flow

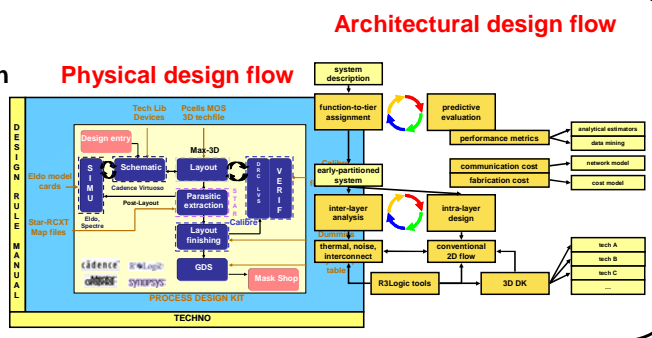
Development of high-level methods to enable the increasingly critical stage of architectural design to exploit the possibilities of 3D integration

**Design flow specification**

**Architectural design flow (high-level models and partitioning methods)**

- 3D thermal model
- High-level 3D interconnect model
- High-level "temperature & noise aware" analog circuit model
- Analog/digital/3D partitioning methods

**Physical design flow**



### WP3: Application and Demonstrator

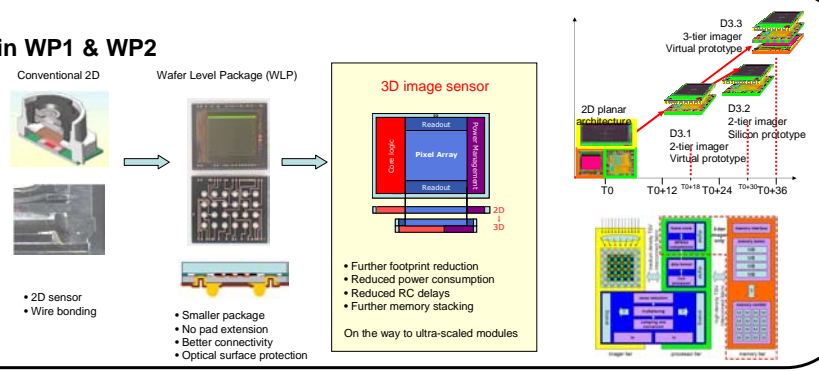
Validation of design flow and process bricks developed in WP1 & WP2

**Silicon prototype**

- 3D integration of an imager on a processing unit
- Test and validation of 3D technology

**Virtual prototyping**

- Partitioning of a 2-stratas virtual demonstrator
  - Stacking of pixel matrix and digital CMOS processor
- Prospective investigation of a 3-stratas virtual circuit
  - Stacking of pixel matrix, CMOS processor and memory



### Information

**Project duration:** March 2009 – February 2012. **Total cost:** 3.3M€. **ANR-PNANO funding:** 1.5M€. **Coordination / contact:** Prof. Ian O'Connor (INL) ian.oconnor@ec-lyon.fr